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EXAMINER	
TURNER, ASHLEY D	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/781,878	SHINOMIYA, KIYOSHI	
	Examiner	Art Unit	
	Ashley D. Turner	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/20/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Referring to claim 1

2. Claims 1,3,5, and 7are rejected under 35 U.S.C. 103(a) as being unpatentable over Ang (US 2004/0221127 A1) in view of Luick (US 2003/0177335 A1).

Referring to claim 1 Ang discloses An inter-computer data transfer method for transferring data between a plurality of computers each including a main storage device i.e. memory controller ([0008] These addresses are then stored in a table which is accessed by the memory controller in order to convert virtual addresses to physical addresses). , A processor i.e. microprocessor for issuing a communication process command and a communication device i.e. peripheral device (in this case Ethernet card) for processing the communication command from said processor and communicating with another one of said computers through a switched network (Pg. 1

[0005] This is particularly important in a symmetric multiprocessing (SMP) environment, where multiple processors have access to and share the same common centralized main memory system). , comprising the step of: each of a transmission section and a reception section of said communication device including a translation look aside buffer for retaining a plurality of translation look aside buffer entries (Pg. 2 [0019] In a preferred embodiment, the microprocessor include an extended version of a conventional translation look-aside buffer (TLB). Like a conventional TLB, the TLB in this invention contains a subset of all mapping from the virtual addresses in the memory to their corresponding physical memory address locations. In a preferred embodiment, each entry in the TLB includes fields to track whether the page represented by the entry is pinned, and the number of times the page has been pinned. Utilizing the TLB, the microprocessor enables user-level code to convert virtual addresses to physical addresses, pin the associated page and convey the physical address to a peripheral device, without making any system calls. The physical address resulting from the translation is conveyed to a peripheral device via bus transactions wherein the address portion of each bus transaction specifies the peripheral device, while the data portion of each bus transaction holds the result of an address translation (i.e. the physical address where the memory access is to occur). As physical addresses are conveyed, the corresponding page in the memory is "pinned". This is reflected in the TLB, as well as the main page table in the main memory.); Ang did not discloses determining, when a communication command including information of that one of the computers which is a sending source is issued from said processor, one of the translation look aside buffer

entries which is to be used in accordance with the computer of the sending source by means of said reception section. The general concept of determining, when a communication command including information of that one of the computers which is a sending source is issued from said processor, one of the translation look aside buffer entries which is to be used in accordance with the computer of the sending source by means of said reception section is well known in the art as taught by Luick. Luick discloses determining, when a communication command including information of that one of the computers which is a sending source is issued from said processor (Pg. 1 [0009] Most modern processors employ some form of pipelining to increase the average number of operations executed per clock cycle, as well as one or more levels of cache memory to provide high-speed access to a subset of data in main memory. Pipelined instruction execution allows subsequent instructions to begin execution before previously issued instructions have finished. Ideally, a new instruction begins with each clock cycle, and subsequently moves through a pipeline stage with each cycle. Even though an instruction may take multiple cycles or pipeline stages to complete, if the pipeline is always full, the processor executes one instruction every cycle.), one of the translation look aside buffer entries which is to be used in accordance with the computer of the sending source by means of said reception section (Pg. 1[0013] Typically, in order to obtain a real address of data for a data reference operation (e.g., a load or store operation), a portion of the virtual address is used to access a table called a translation look aside buffer (TLB). The TLB is typically N-way set associative, providing N possible real address entries corresponding to the virtual address. A TLB lookup

requires that the N entries be retrieved from the TLB, that each entry be compared to the virtual address, and that the real address corresponding to the matched entry be selected. These operations may require multiple clock cycles). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Ang to include determining, when a communication command including information of that one of the computers which is a sending source is issued from said processor, one of the translation look aside buffer entries which is to be used in accordance with the computer of the sending source by means of said reception section in order to improved techniques for dealing with pipeline address conflicts.

Referring to claim 3

3. Referring to claim 3 Ang and Luick disclose all the limitations of claim 3 which is described above. Ang also discloses wherein the number of communication commands to be processed simultaneously to the same destination computer from the computer of the sending source is limited by said communication device (Pg.9 [0064] The number of pages which may be pinned down by any single user-level job or process, as well as the total number of pages which may be pinned down, is preferably capped at operator programmable levels. In a preferred embodiment of the present invention, an attempt to translate a virtual address to a to physical address i and pin down the associated page in the memory will fail if either of these two counters is already at its maximum value. Accordingly, before any Trans_and_pin or Trans_and_pin_only transaction is complete,

the counters are checked to see if they are at their maximum allowable value. If so, the physical addresses are not passed to the peripheral device or to the physical address register and the pages are not pinned down. Instead, the failure status of executing the trans_and_pin instruction is reflected in the <outcome> field of the instruction).

Referring to claim 5

Referring to claim 5 Ang discloses An inter-computer network system, comprising: a plurality of computers connected to each other; each of said computers including a main storage device, i.e. memory controller ([0008] These addresses are then stored in a table which is accessed by the memory controller in order to convert virtual addresses to physical addresses). A processor i.e. microprocessor for issuing a communication processing command, and a communication device i.e. peripheral device (in this case Ethernet card) for processing the communication command from said processor and communicating with another one of said computers through said switching network; said communication device including a transmission section for transmitting a communication to and a reception section for receiving a communication to said switched network (Pg. 2 [0010] The invention includes a memory system and a set of user-level instructions, i.e. instructions that are callable from user-level code, for converting virtual addresses to physical, addresses without requiring a system call. In a preferred embodiment of the invention, the memory system includes a memory, a memory controller, a microprocessor, and one or more peripheral devices. In a preferred embodiment, the system of the present invention uses an extended version of

a conventional translation look-aside buffer (TLB) implemented in the microprocessor to allow user-level code running on the microprocessor to convert virtual addresses to physical addresses, pin the associated page, and convey the physical address to a peripheral device, without making any system calls. The result of the translation is conveyed to a peripheral device via a bus transaction wherein the address portion of the bus transaction targets the peripheral device, while the data portion of the bus transaction holds the result of the translation (i.e. the physical address where the memory access is to occur). The system further allows user-level code to unpin a previously pinned page once the peripheral access has completed.); each of said transmission section and said reception section including a translation look aside buffer for retaining a plurality of translation look aside buffer entries (Pg. 2 [0019] The microprocessor include an extended version of a conventional translation look-aside buffer (TLB). Like a conventional TLB, the TLB in this invention contains a subset of all mapping from the virtual addresses in the memory to their corresponding physical memory address locations. In a preferred embodiment, each entry in the TLB includes fields to track whether the page represented by the entry is pinned, and the number of times the page has been pinned. Utilizing the TLB.). Ang did not discloses processor issuing the communication command which includes information of that one of the computers which is a sending source; said reception section determining one of the translation look aside buffer entries which is to be used in accordance with the computer of the sending source. The general concept of processor issuing the communication command which includes information of that one of the computers which is a sending

source; said reception section determining one of the translation look aside buffer entries which is to be used in accordance with the computer of the sending source is well known in the art as taught by Luick. Luick discloses processor issuing the communication command which includes information of that one of the computers which is a sending source (Pg. 1 [0009] Most modern processors employ some form of pipelining to increase the average number of operations executed per clock cycle, as well as one or more levels of cache memory to provide high-speed access to a subset of data in main memory. Pipelined instruction execution allows subsequent instructions to begin execution before previously issued instructions have finished. Ideally, a new instruction begins with each clock cycle, and subsequently moves through a pipeline stage with each cycle. Even though an instruction may take multiple cycles or pipeline stages to complete, if the pipeline is always full, the processor executes one instruction every cycle.); said reception section determining one of the translation look aside buffer entries which is to be used in accordance with the computer of the sending source (Pg. 1[0013] Typically, in order to obtain a real address of data for a data reference operation (e.g., a load or store operation), a portion of the virtual address is used to access a table called a translation look aside buffer (TLB). The TLB is typically N-way set associative, providing N possible real address entries corresponding to the virtual address. A TLB lookup requires that the N entries be retrieved from the TLB, that each entry be compared to the virtual address, and that the real address corresponding to the matched entry be selected. These operations may require multiple clock cycles). It would have been obvious to one of ordinary skill in the art at the time of the invention to

modify Ang to include processor issuing the communication command which includes information of that one of the computers which is a sending source; said reception section determining one of the translation look aside buffer entries which is to be used in accordance with the computer of the sending source in order to improved techniques for dealing with pipeline address conflicts.

Referring to claim 7

Referring to claim 7 Ang and Luick discloses all the limitations of claim 7 which is described above. Ang also discloses wherein said communication apparatus limits the number of communication commands to be processed simultaneously to the same destination computer from the computer of the sending source. (Pg.9 [0064] The number of pages which may be pinned down by any single user-level job or process, as well as the total number of pages which may be pinned down, is preferably capped at operator programmable levels. In a preferred embodiment of the present invention, an attempt to translate a virtual address to a to physical address i and pin down the associated page in the memory will fail if either of these two counters is already at its maximum value. Accordingly, before any Trans_and_pin or Trans_and_pin_only transaction is complete, the counters are checked to see if they are at their maximum allowable value. If so, the physical addresses are not passed to the peripheral device or to the physical address register and the pages are not pinned down. Instead, the failure status of executing the trans_and_pin instruction is reflected in the <outcome> field of the instruction).

4. Claims 2,4,6,8,9,10,and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ang (US 2004/0221127 A1) in view of Luick (US 2003/0177335 A1) further in view of Hayes (US 5,497,480).

Referring to claim 2

Referring to claim 2, Ang and Luick disclose all the limitations of claim 2 which is described above. Ang did not disclose wherein said transmission section of said communication device produces a communication packet including the information of the computer of the sending source and transmits the communication packet to another one of said computers. The general concept of transmission section of said communication device produces a communication packet including the information of the computer of the sending source and transmits the communication packet to another one of said computers is well known in the art as taught by Hayes. Hayes discloses transmission section of said communication device produces a communication packet including the information of the computer of the sending source and transmits the communication packet to another one of said computers (Col.2 lines 23-34 A method and apparatus for removing a page table entry from a plurality of translation look aside buffers ("TLB's") coupled to a plurality of processors in a multiprocessor system is disclosed. The method comprises the steps of issuing a request packet by a first

controller of the first TLB to remove the page table entry from the first TLB; sending the request packet to the packet-switched bus to be broadcast to a second controller coupled to a second TLB with the request packet specifying a predetermined source, the first address mode and process identification; receiving the request packet by the second controller on the packet-switched bus). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Ang to include transmission section of said communication device produces a communication packet including the information of the computer of the sending source and transmits the communication packet to another one of said computers in order to provide a broadcast page removal scheme for all the processors on a multiprocessor computer system.

Referring to claim 4

Referring to claim 4 Ang and Luick disclose all the limitations of claim 4 which is described above. Ang did not disclose wherein an identification number of a processing command in the computer of the sending source is applied to a communication packet by said communication device, and for different communication packets which have the same identification number of the processing command, the same translation look aside buffer entry is used by said reception section of said communication device. The general concept of wherein an identification number of a processing command in the computer of the sending source is applied to a communication packet by said communication device, and for different communication packets which have the same identification number of the processing command, the same translation look aside buffer

entry is used by said reception section of said communication device is well known in the art as taught by Hayes. Hayes discloses wherein an identification number i.e. TLB entry of a processing command in the computer of the sending source is applied to a communication packet by said communication device, and for different communication packets which have the same identification number of the processing command, the same translation look aside buffer entry is used by said reception 10 section of said communication device (Col.2 lines 23-34 A method and apparatus for removing a page table entry from a plurality of translation look aside buffers ("TLB's") coupled to a plurality of processors in a multiprocessor system is disclosed. The method comprises the steps of issuing a request packet by a first controller of the first TLB to remove the page table entry from the first TLB; sending the request packet to the packet-switched bus to be broadcast to a second controller coupled to a second TLB with the request packet specifying a predetermined source, the first address mode and process identification; receiving the request packet by the second controller on the packet-switched bus). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Ang to include wherein an identification number of a processing command in the computer of the sending source is applied to a communication packet by said communication device, and for different communication packets which have the same identification number of the processing command, the same translation look aside buffer entry is used by said reception section of said communication device in order to provide a broadcast page removal scheme for all the processors on a multiprocessor computer system.

Referring to claim 6

Referring to claim 6 Ang and Luick disclose all the limitations of claim 6 which is described above. Ang did not disclose wherein said transmission section produces a communication packet including the information of the computer of the sending source and transmits the communication packet to another one of said computers. The general concept of transmission section produces a communication packet including the information of the computer of the sending source and transmits the communication packet to another one of said computers is well known in the art as taught by Hayes. Hayes discloses transmission section produces a communication packet including the information of the computer of the sending source and transmits the communication packet to another one of said computers. (Col.2 lines 23-34 A method and apparatus for removing a page table entry from a plurality of translation look aside buffers ("TLB's") coupled to a plurality of processors in a multiprocessor system is disclosed. The method comprises the steps of issuing a request packet by a first controller of the first TLB to remove the page table entry from the first TLB; sending the request packet to the packet-switched bus to be broadcast to a second controller coupled to a second TLB with the request packet specifying a predetermined source, the first address mode and process identification; receiving the request packet by the second controller on the packet-switched bus). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Ang to include transmission section produces a communication packet including the information of the computer of the sending source

and transmits the communication packet to another one of said computers in order to provide a broadcast page removal scheme for all the processors on a multiprocessor computer system.

Referring to claim 8

Referring to claim 8 Ang and Luick disclose all the limitations of claim 8 which is described above. Ang did not disclose wherein said communication apparatus applies an identification number of a processing command in the computer of the sending source to a communication packet, and said reception section uses the same translation look aside buffer entry for different communication packets which have the same identification number of the processing command. The general concept of communication apparatus applies an identification number of a processing command in the computer of the sending source to a communication packet, and said reception section uses the same translation look aside buffer entry for different communication packets which have the same identification number of the processing command is well known in the art as taught by Hayes. Hayes discloses wherein said communication apparatus applies an identification number of a processing command in the computer of the sending source to a communication packet, and said reception section uses the same translation look aside buffer entry for different communication packets which have the same identification number of the processing command. (Col.2 lines 23-34 A method and apparatus for removing a page table entry from a plurality of translation

look aside buffers ("Tab's") coupled to a plurality of processors in a multiprocessor system is disclosed. The method comprises the steps of issuing a request packet by a first controller of the first TLB to remove the page table entry from the first TLB; sending the request packet to the packet-switched bus to be broadcast to a second controller coupled to a second TLB with the request packet specifying a predetermined source, the first address mode and process identification; receiving the request packet by the second controller on the packet-switched bus). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Nag to include communication apparatus applies an identification number of a processing command in the computer of the sending source to a communication packet, and said reception section uses the same translation look aside buffer entry for different communication packets which have the same identification number of the processing command in order to provide a broadcast page removal scheme for all the processors on a multiprocessor computer system.

Referring to claim 9

Referring to claim 9 Ang and Luick discloses all the limitations of claim 9 which is described above. Ang also discloses transmission section of said communication device extracts a communication command from said main storage device in accordance with an instruction from said processor (Pg.1 [0006] a microprocessor may execute user-level code which requires an Ethernet/network card to retrieve some data from several different virtual address locations (which correspond with actual physical address

locations in the memory) and pass that data out over the network to which the computer system is connected. When this is encountered in user-level code, the peripheral hardware device must receive physical addresses in order to perform the data send command. Accordingly, whenever this function is encountered in user-level code, the microprocessor will perform a system call in order to convert the virtual addresses in the instruction set into physical addresses. These physical addresses are then passed to the peripheral device so that the peripheral device knows where (which physical addresses) to access the data from in the memory. Therefore, in this example, the virtual address locations from which the data is to be retrieved must be converted into actual physical address locations in the memory so the physical addresses can be transfer red to the peripheral hardware device (in this case, the Ethernet card), converts a logical address of data of the sending source in the communication command into a physical address, extracts transmission data from said main storage device the microprocessor will perform a system call in order to convert the virtual addresses in the instruction set into physical addresses. These physical addresses are then passed to the peripheral device so that the peripheral device knows where (which physical addresses) to access the data from in the memory. Therefore, in this example, the virtual address locations from which the data is to be retrieved must be converted into actual physical address locations in the memory so the physical addresses can be transfer red to the peripheral hardware device (in this case, the Ethernet card)). Ang did not disclose produces a communication packet from the extracted data and the communication command and transmits the communication packet to the destination

computer. The general concept of a communication packet from the extracted data and the communication command and transmits the communication packet to the destination computer is well known in the art as taught by Hayes. Hayes discloses a communication packet from the extracted data and the communication command and transmits the communication packet to the destination computer (Abstract The multiprocessor computer system includes at least two processors coupled to a packet-switched bus. Page table entries are removed from a plurality of TLBs in the multiprocessor computer system by first broadcasting a demap request packets on the packet -switched bus in response to one of the processors requesting that a page table entry be removed from its associated TLB. The demap request packet includes a virtual address and context information specifying this page table entry. Controllers reply to the demap request packet by sending a first reply packet to the controller that sent the original demap request packet to indicate receipt of the demap request packets. If a controller removes the page table entry from its associated TLB, that controller sends a second demap reply packet to indicate that the page table entry has been removed from its associated TLB. It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Ang to include a communication packet from the extracted data and the communication command and transmits the communication packet to the destination computer in order to provide a broadcast page removal scheme for all the processors on a multiprocessor computer system.

Referring to claim 10

Referring to claim 10 Ang and Luick discloses all the limitations of claim 10, which is, describe above. Ang did not disclose wherein said reception section of said communication device receives a communication packet from said switched network, converts a destination logical address into a destination physical address for said main storage device and writes data in the communication packet into the destination physical address. The general concept of wherein said reception section of said communication device receives a communication packet from said switched network, converts a destination logical address into a destination physical address for said main storage device and writes data in the communication packet into the destination physical address is well known in the art as taught by Hayes. Hayes discloses wherein said reception section of said communication device receives a communication packet from said switched network (Col.2 lines 27 - issuing a request packet by a first controller of the first TLB to remove the page table entry from the first TLB; sending the request packet to the packet-switched bus to be broadcast to a second controller coupled to a second TLB with the request packet specifying a predetermined source, the first address mode and process identification; receiving the request packet by the second controller on the packet-switched bus; checking by the second controller to determine whether the second TLB contains the page table entry by comparing the first mode address and process identification; completing any pending operations for the second processor; removing the page table entry from the second TLB by the second controller if the page table entry is contained in the second TLB; issuing a reply packet by the second controller to indicate completion to the first controller; sending the reply Packet

to the Packet-switched bus to be forwarded to the first controller with the reply packet identifying the source.) converts a destination logical address into a destination physical address for said main storage device and writes data in the communication packet into the destination physical address (Col. 3 lines 13-21 Processor 110 is coupled to system bus 100 through cache controller 111 and bus watcher 112. Processor 110 also utilizes translation look aside buffer ("TLB") such as I/O TLB 114 or system TLB 113 to store its already translated virtual-to- physical address mapping in conjunction with its cache (not shown). Processors 120 and 130 are similarly coupled to system bus 100 through their respective cache controllers and bus watchers. When processor 110 needs to demap virtual-to- physical mapping for one or more virtual pages, its cache controller 111 issues a broadcast demap request packet onto system bus 100 through bus watcher 112. As other bus watchers 122 and 132 receive the demap request packet they forward the demap request packet to their respective cache controllers 121 and 131 for execution). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Ang to include wherein said reception section of said communication device receives a communication packet from said switched network, converts a destination logical address into a destination physical address for said main storage device and writes data in the communication packet into the destination physical address in order to provide a broadcast page removal scheme for all the processors on a multiprocessor computer system.

Referring to claim 11

Referring to claim 11, Ang and Luick disclose all the limitations of claim 11, which is described above. Ang also discloses wherein a destination computer number for setting a destination computer number for the communication command, a process number representative of a process of a communication opposite party for setting the destination process number of the communication command (Pg. 2 [0012] In a preferred embodiment, the present invention also tracks the total number of pages which are in use by peripheral devices, i.e., being written to or read from in the memory by a peripheral connected to the computer system in which the present invention is implemented. Pages which are in use per transaction or user-level job are "pinned down" and a total count of the number of pinned memory pages per transaction or user-level job is maintained in order to ensure that a single transaction or user-level job does not use too much memory space, thereby halting other processes from operating concurrently. In a preferred embodiment, total pages pinned counts per transaction or user-level job, as well as overall pinned pages counts system wide in the entire memory are maintained. These counts are compared to allowable transaction or user-level job maximum and overall system maximum values. In this way, no one transaction or user-level job has access to more than a predetermined maximum number of memory locations and the overall size of the memory allocated to concurrently executing transactions may also be limited). Ang did not discloses a destination logical address representative of a writing destination of the data in the destination process for setting the destination logical address for the packet, a data length for setting a length of data

of the packet, a sending source computer number for identification of a sending source for setting a sending source computer number of the communication command, the communication packet includes a command code for setting a communication command, and data to be written into destination. The general concept of a destination logical address representative of a writing destination of the data in the destination process for setting the destination logical address for the packet, a data length for setting a length of data of the packet, a sending source computer number for identification of a sending source for setting a sending source computer number of the communication command, the communication packet includes a command code for setting a communication command, and data to be written into destination is well known in the art as taught by Hayes. Hayes discloses a destination logical address representative of a writing destination of the data in the destination process for setting the destination logical address for the packet (Col. 3 lines 13-21 Processor 110 is coupled to system bus 100 through cache controller 111 and bus watcher 112. Processor 110 also utilizes translation look aside buffer ("TLB") such as I/O TLB 114 or system TLB 113 to store its already translated virtual-to- physical address mapping in conjunction with its cache (not shown). Processors 120 and 130 are similarly coupled to system bus 100 through their respective cache controllers and bus watchers. When processor 110 needs to demap virtual-to- physical mapping for one or more virtual pages, its cache controller 111 issues a broadcast demap request packet onto system bus 100 through bus watcher 112. As other bus watchers 122 and 132 receive the demap request packet they forward the demap request packet to their respective cache

controllers 121 and 131 for execution), a data length for setting a length of data of the packet, a sending source computer number for identification of a sending source for setting a sending source computer number of the communication command, the communication packet includes a command code for setting a communication command, and data to be written into destination. (Col.2 lines 27 - issuing a request packet by a first controller of the first TLB to remove the page table entry from the first TLB; sending the request packet to the packet-switched bus to be broadcast to a second controller coupled to a second TLB with the request packet specifying a predetermined source, the first address mode and process identification; receiving the request packet by the second controller on the packet-switched bus; checking by the second controller to determine whether the second TLB contains the page table entry by comparing the first mode address and process identification; completing any pending operations for the second processor; removing the page table entry from the second TLB by the second controller if the page table entry is contained in the second TLB; issuing a reply packet by the second controller to indicate completion to the first controller; sending the reply Packet to the Packet-switched bus to be forwarded to the first controller with the reply packet identifying the source). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Ang to include a destination logical address representative of a writing destination of the data in the destination process for setting the destination logical address for the packet, a data length for setting a length of data of the packet, a sending source computer number for identification of a sending source for setting a sending source computer number of the

communication command, the communication packet includes a command code for setting a communication command, and data to be written into destination to provide a broadcast page removal scheme for all the processors on a multiprocessor computer system.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ashley d. Turner whose telephone number is 571-270-1603. The examiner can normally be reached on Monday thru Friday 7:30a.m. - 5:00p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached at 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 571-270-2603.

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Patent Examiner:

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